S.N.: 10/651,210
Art Unit: 2686

REMARKS

Claims 1-25 are currently pending in this patent application. Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Pehlke et al. (US 2005/0032488 A1). This rejection is respectfully disagreed with, and is traversed below.

An element of each of the independent claims 1, 9, 17 and 21 is, as in claim 1:

> "compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, **and the current output power level of the power amplifier module**." (emphasis added)

There is no similar teaching in Pehlke et al., and no suggestion of the claimed subject matter. This fact alone should be sufficient to traverse the rejection applied under 35 U.S.C. 102(e).

Independent claim 20 recites in part that a RF power amplifier is contained within a package and is operable:

> "**over a range of output power levels specified by a value of a power control signal** that is one of applied to a first input of the package and generated internally to the package, the RF power amplifier comprising at least one output transistor having an input coupled to second input of the package for receiving an input RF signal and an output coupled to an output of the package for outputting an amplified RF signal, the RF power amplifier further comprising circuitry integrated with the at least one output transistor for automatically compensating the RF amplifier for impedance variations appearing at the first output, the circuitry comprising detection circuitry for generating detection signals indicative of current flowing through the at least one output transistor and of a voltage appearing at the output of the at least one output transistor, and further comprising load line compensation circuitry responsive to the detection signals **and to the power control signal** for maintaining a desired output linearity of the amplified RF signal."

As is stated at page 9, lines 10-13, of the instant specification:

> "In addition, the power detector 30, 32 outputs are matched to the internal (or external) reference voltage Vref. The value of Vref is proportional to the desired output power from the PA. That is, during normal operation the value of Vref varies up and down, depending on the PA output power."

Pehlke et al. do make a reference to VREF, but in the following context (see, for example, paragraph 0078):

> "The voltage drop across the reference regulating transistor 40A, e.g., the drain-to-source drop if 40A is a FET, is sensed and amplified by a factor A_{VREF} by amplifier 60, and compared against the corresponding voltage drop across the PA's regulating transistor 40B, which is sensed and amplified similarly by a factor A_{VPA} by amplifier 62. These sensed and amplified voltages, which represent the relative instantaneous headroom to the supply voltage upper rail of each branch, are then compared in amplifier 64 and used to lock the loop by driving the gate of transistor 40B, which regulates current into PA 12.

Reference can also be made to paragraph 0080. Clearly the VREF of Pehlke et al. is not equivalent to the Vref or VREF disclosed in the instant patent application.

In rejecting claims 1, 9, 17, 20 and 21 the Examiner refers to paragraphs 0042, 0068, 0081, 0082 of Pehlke et al. for purportedly teaching the "current output power level of the power amplifier module" (Office Action at page 3, lines 6, 7).

What is actually stated in these paragraphs is the following:

> [0042] In operation, the AM_{IN} signal is generated as, or converted to, a voltage-mode signal applied to the non-inverting input of the control amplifier 16, which may, for example, be an operational amplifier. The control amplifier 16 generates a control voltage based on the difference between the AM_{IN} signal and a feedback signal taken from the supply current path of the power amplifier 12. The control voltage sets the gate bias for the pass transistor 16, which in turn sets the magnitude of the supply current I_{PA} provided to the power amplifier 12.
>
> [0068] Note that detection circuit 48 can be configured to generate a detection signal in proportion to the detected voltage difference(s), and the control circuit 50 can be configured to generate a compensation signal responsive thereto. For

example, in a burst-mode transmission configuration, circuit 46 preferably is configured to sense changes during active signal transmission but defer its compensating adjustments until a time when there is no active transmission. For example, circuit 46 may detect voltage discrepancies between $V_{IN'}$ and V_{PA} during a given transmit burst, and then update the compensation signal during the non-transmit time in advance of the next burst. Doing so avoids making compensation changes during an active transmission. Of course, some types of signal transmission may be tolerant of such changes during live transmission and it should be understood that the deferred adjustment approach described here is a non-limiting implementation detail.

[0081] The PA DC current, I_{PA}, is thereby a scaled version of the reference current, I_{REF}, proportional to the ratio of reference resistance (fixed and known) to PA DC resistance (variable and unknown). No matter what the value of the PA DC resistance R_{PA}, the headroom and linearity of the PA regulator is maintained while still modulating the DC current of the PA. As the PA DC current increases or decreases in response to changing antenna impedance, the forward available power out of the mismatched antenna will vary, but the maximum PA DC resistance is not allowed to force a headroom clipping distortion.

[0082] Thus, this embodiment enables a known reference current to be mirrored by a dynamically adjusting scale factor in closed loop to overcome variation that would otherwise degrade headroom and result in nonlinear clipping distortion of the regulated current to the PA. This closed loop continuous analog headroom mirroring is one embodiment of mirroring a reference current to the supply current of the PA without suffering headroom-clipping distortion. Similar variants of this embodiment may be implemented in a discrete manner, such that the feedback stages N_{FBPA} and N_{FBREF} may be adjusted in discrete steps in response to a known detection of headroom degradation, similar to the adjustment of PA bias, physical size, and/or output match described previously. (Note that each such feedback stage may provide gain control via a passive resistor/capacitor network as illustrated, but those skilled in the art will recognize that other feedback network configurations can be used, depending on the needs of the particular design at hand.)

These specific paragraphs of Pehlke et al. are not seen to disclose or suggest the subject matter of the independent claims, e.g., as in claim 1: "compensation circuitry for controlling the generation of a plurality of power amplifier bias current and bias voltage signals to have values that are a function of the values of the first and second detection signals, **<u>and the current output power level of the power amplifier module</u>**."

All of the independent claims are allowable over Pehlke et al. and, thus, all of the dependent claims are allowable as well for at least this one reason alone.

Note further that this patent application claims (e.g., as in claim 1), "compensation circuitry for controlling the **generation of a plurality of power amplifier bias current and bias voltage signals**". This subject matter as well is not seen to be expressly disclosed or suggested by Pehlke et al., such as in paragraphs 0066, 0079 and 0080, as stated by the Examiner.

The Examiner is respectfully requested to reconsider and remove the rejections of the claims under 35 U.S.C. 102(e) based on Pehlke et al., and to allow all of the pending claims 1-25 as originally filed. An early notification of the allowability of claims 1-25 is earnestly solicited.

Respectfully submitted:

Harry Smith 12-06-2005

Harry F. Smith
Reg. No.: 32,493

Customer No.: 29683

HARRINGTON & SMITH, LLP
4 Research Drive
Shelton, CT 06484-6212

Telephone: (203)925-9400
Facsimile: (203)944-0245
email: hsmith@hspatent.com

Date

S.N.: 10/651,210
Art Unit: 2686

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450.

December 6, 2005

Date

Name of Person Making Deposit